



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,616	02/11/2002	Timothy A. Lewis	01-1002	5952
7590	07/07/2005		EXAMINER	
Loren H. McRoss PHOENIX TECHNOLOGIES LTD 411 East Plumeria Drive San Jose, CA 95134			CHAI, LONGBIT	
			ART UNIT	PAPER NUMBER
			2131	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,616	LEWIS, TIMOTHY A.	
Examiner	Art Unit		
Longbit Chai	2131		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 26 August 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) _____ is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 11 February 2002 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date, _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____.

DETAILED ACTION

Priority

1. No claim for priority has been made in this application.

The effective filing date for the subject matter defined in the pending claims in this application is 2/11/2002.

Drawings

The drawings are objected to because Element 43 of Figure 3 should be "BIOS COPIES ITSELF INTO SHADOW RAM" instead of "BIOS COPIES ITSELF INTO DRAM" according to paragraph [0042] in specification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A person shall be entitled to a patent unless –

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexander (Patent Number: 6188602), in view of Bealkowski (Patent Number: 6878256).

As per claim 1, 7 and 13, Alexander teaches a system having secure system firmware, comprising:

a central processing unit (CPU) (Alexander: Figure 1 Element 102);
sets LOCK bits associated with the registers of the flash memory that holds the BIOS, boots a computer operating system, monitors attempted writes to locked registers of the flash memory (Alexander: Column 3 Line 37 – 61), and if a write operation to a locked register is detected, generates an interrupt that indicates an attempt to tamper

with the system firmware (Alexander: Column 5 Line 21 – 25 and Column 5 line 53 – 67);

Alexander does not disclose expressly that the BIOS image in the flash memory incorporated with BIOS RD/WR access protection by using LOCK register and SMI interrupt could be in shadow RAM instead.

However, Bealkowski teaches:

a dynamic random access memory (DRAM) coupled to the CPU that comprises a shadow random access memory (RAM) including one or more registers whose attributes are separately configurable (Bealkowski, Column 13 Line 12 – 15); and system firmware that when the system is reset, initializes the DRAM and the shadow RAM (Bealkowski, Column 13 Line 12 – 15), copies itself into the shadow RAM (Bealkowski, Column 13 Line 63 – 66);

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Bealkowski within the system of Alexander because (a) Alexander teaches a mechanism to provide RD/WR access protection to BIOS image in the flash memory by using LOCK register and SMI interrupt, and (b) Bealkowski teaches providing a significant performance improvement by copying the BIOS image into the shadow RAM, which has normally faster access speed (Bealkowski: see for example, Column 13 Line 32 – 37).

Therefore, Alexander in view of Bealkowski teaches:

sets LOCK bits associated with the registers of the shadow RAM, boots a computer operating system, monitors attempted writes to locked registers of the shadow

RAM, and if a write operation to a locked register is detected, generates an interrupt that indicates an attempt to tamper with the system firmware.

As per claim 2, 8 and 14, Alexander as modified teaches the interrupt that is generated is selected from a group consisting of a system management interrupt (SMI), a non-maskable interrupt (NMI) and a general-purpose interrupt (Alexander: Column 5 Line 58 – 61).

As per claim 3, 9 and 15, Alexander as modified teaches the system firmware enables generation of the interrupt before initiating operating system code and after all modifications to the shadow RAM are complete (Alexander: Column 1 Line 55 – 56: Alexander teaches lock critical portion that holds BIOS image to prevent it from being corrupted “during initialization” – i.e. enables generation of the interrupt before initiating operating system code and after all modifications to the shadow RAM are complete – i.e. the interrupt can be generated successfully during the initialization).

As per claim 4, 10 and 16, Alexander as modified teaches the system firmware begins execution when the interrupt is generated and performs a desired behavior (Alexander: Column 5 Line 21 – 25 and Column 5 Line 58 – 67).

As per claim 5, 11 and 17, Alexander as modified teaches the desired behavior includes an security alert, remote administrator signaling, logging of an event, or

ignoring of the event and resuming operation (Alexander: Column 5 Line 21 – 25 and Column 5 Line 58 – 67 and Column 3 Line 56 – 57).

As per claim 6, 12 and 18 – 20, Alexander as modified teaches the system firmware is selectively configured to programmatically enable and disable write access to a selected shadow RAM register (Alexander: Column 3 Line 40 – 41), programmatically enable and disable read access to a selected shadow RAM register (Alexander: Column 3 Line 40 – 41), and programmatically enable and disable cacheability of a shadow RAM register (Alexander: Column 3 Line 40 – 41: the combination RD/WR disable of LOCK register as taught by Alexander is equivalent to disable cacheability of a shadow RAM register).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Longbit Chai whose telephone number is 571-272-3788. The examiner can normally be reached on Monday-Friday 8:00am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Longbit Chai
Examiner
Art Unit 2131



LBC



AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100